## In re U.S. Patent Application of OOSAWA et al. Serial Number: 10/615,787 Filed: July 10, 2003 For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE Attorney Docket No. HITA.0413

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Honorable Assistant Commissioner for Patents Washington, D.C. 20231

## INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, this Information Disclosure Statement is submitted in the above-identified patent application. A listing of documents to be published on the face of any patent granted from this application is submitted herewith on Form PTO-1449. Any other documents or information submitted for consideration by the Examiner are listed in this paper. A copy of each U.S. and foreign patent, or each publication or portion thereof listed or herein identified, is submitted herewith.

## **CERTIFICATION**

This Information Disclosure Statement is submitted after three months from the filing date of the above-identified U.S. patent application and after the mailing date of the first Office Action on the merits of the above-identified application. The fee required under 37 C.F.R. 1.97(c) is submitted herewith.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

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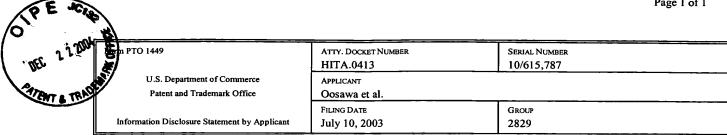
Respectfully submitted,

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REED SMITH LLP 3110 Fairview Park Drive Suite 1400 Falls Church, Virginia 22042 (703) 641-4200 December 22, 2004



## U.S. Patent Documents

Examiner Initial	Cited By Examiner in Parent	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
		5,900,739	5/4/1999	Gaglany			9/24/1996
		6,298,458	10/2/2001	Cranford et al.			1/4/1999
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Foreign Patent Documents

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Examiner	Cited By	DOCUMENT	FILING DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
Initial	Examiner	Number		<u> </u>			YES	No
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Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

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